INSIDER

ASIX®

Monitoring device for microprocessor and FPGA based applications

1. INSIDER

INSIDER is cost effective and powerful tool for electronic application development.

2. Usage

INSIDER can be used to monitor state of program in applications with any type of microcontroller (Microchip PIC, Atmel, Motorola, ...), state of FPGA device or any other digital circuit operating at voltage levels of 3 or 5 V. Main advantage of INSIDER is significant increase of efficiency of work while debugging realtime applications, also in cases when no emulator or other debugging tool is available. Due to low price, minimal requirements for monitored system and time savings it lowers total price of application development and thus increases customers satisfaction.

3. Features

- displays any user data of 4/8/16 bits in hexadecimal format on a 4 digit LED display
- input signals:
  - DATA data
  - CLK clock
  - EN enable (optional)
- configurable active clock edge (rising/falling)
- fully configurable EN input:
  - used/unused
  - clock enable / data strobe (latch)
  - active level selection low/high
- high speed (up to 50 MHz)
- status LED indicators for DATA, CLK and EN inputs
- CMOS – 3 V, 5 V / TTL / LVT compatible inputs
- Schmitt triggers on input signals
- inputs are immune to voltage leakage from application to INSIDER and back
- power LED indicator
- power supply 9 V DC, 300 mA

4. Function description

INSIDER allows the application to display 4/8/12/16 bits of data transferred using CLK, DATA and optionally EN signals, for monitoring of behaviour of microcontroller program in real time.

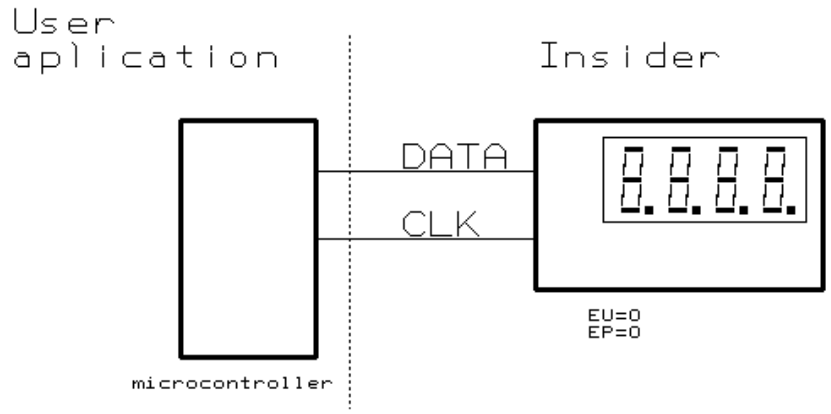
The core of INSIDER is formed of 16-bit shift register, 16-bit latch, hexadecimal decoder and a display (see Fig. 1).

INSIDER supports 3 operational modes:

- 2-wire mode data acquisition of 4/8/12/16 bits
- 3-wire mode, EN is used as clock enable
- 3-wire mode, EN used for data strobe

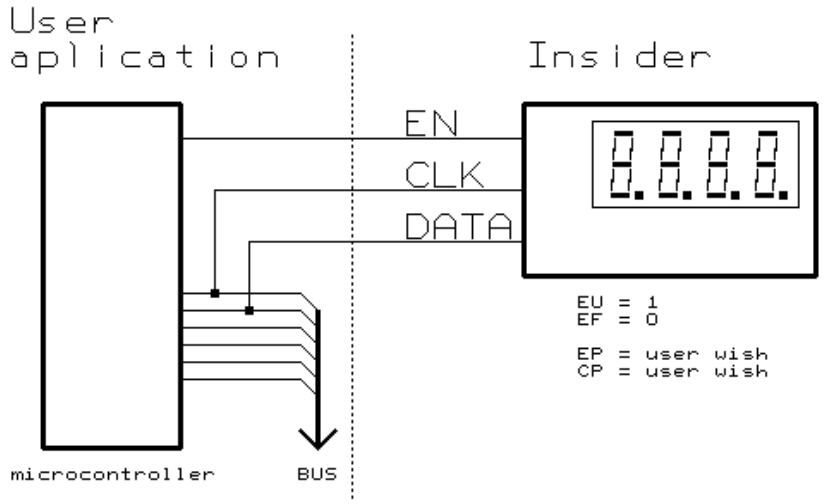
If there are only 2 free wires available in debugged application, it is possible to use 2-wire mode. In this case only DATA and CLK signals are connected to application pins. By using a simple subroutine on desired place of user program the data to be displayed are sent to INSIDER (see Fig. 2).

Fig. 1: 2-wire mode



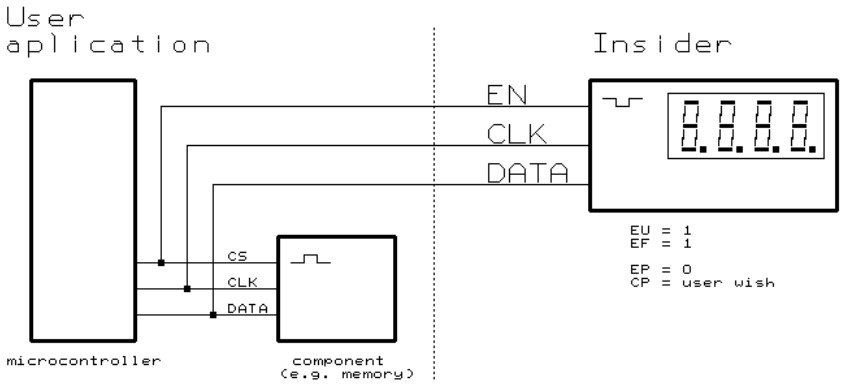
For applicatios having only 1 free output and 2 other outputs which may be used under certain circumstances (e.g. a bus) 3-wire mode with EN as clock enable is available. CLK and DATA are connected to data bus (see Fig. 3).

Fig. 2: 3-wire connection with clock enable signal



If there are no free output pins available but there are some components active in certain logical level of a signal (typically CS), it is possible to use 3-wire connection when EN is shared with this signal (CS) and it is used as data strobe (see Fig.4).

Fig. 3: 3-wire connection in latch mode



The polarity of EN signal is to be set oposite to presented shared signal (CS).

5. DIP switch configuration

CP (Clock polarity) selects polarity of CLK signal.

CP=0 falling edge (the data is transferred to register on falling edge of CLK signal)

CP=1 ririsng edge (the data is transferred to register on frising edge of CLK signal)

EU (Enable used) determines whether EN signal is used

EU=0 EN signal is ignored

EU=1 EN signal is to be used (see examples above)

Note If EU=0 set also EP=0 to enable INSIDER to receive the data

EF (Enable function) determines whether EN signal is used as clock enable or data strobe.

EF=0 EN signal is used as clock enable

EF=1 EN signal is used as data strobe

EP (Enable polarity) determines polarity of EN signal. The meaning of the signal is affected by EU and EF switches.

EP=0 data is received or clock is enabled when EN=0

EP=1 data is received or clock is enabled when EN=1

DIP switch settings	EN signal	function
EU=0 EF=0 EP=0	x	data is continuously received by every period of CLK
EP=1	x	new data is ignored (last state is kept – memory function)
EF=1 EP=0	x	data is continuously received by every period of CLK
EP=1	x	new data is ignored (last state is kept – memory function)
EU=1 EF=0 EP=0	EN=0	data is received by every period of CLK signal
	EN=1	new data is ignored, change to CLK signal will not affect state of INSIDER
EU=1 EF=0 EP=1	EN=0	new data is ignored, change to CLK signal will not affect state of INSIDER
	EN=1	data is received by every period of CLK signal
EU=1 EF=1 EP=0	EN=0	data is received by every period of CLK signal
	EN=1	latch function – by every period of CLK signal new data is received but the display keeps old data (valid upon last EN=0)
EU=1 EF=1 EP=1	EN=0	latch function – by every period of CLK signal new data is received but the display keeps old data (valid upon last EN=1)
	EN=1	data is received by every period of CLK signal

6. Operational mode selection

6.1 2-wire mode acquisition of 4/8/12/16 bits of data

If DIP switch EU=0 and EP=0, 2-wire mode with only CLK and DATA singals is selected. In this mode the data is continuously captured upon every period of CLK signal and display in MSB to LSB order (last captured bit is the least significant bit of segment SEG1).

This mode may be used to capture 4/8/12/16-bit data sequences.

If 4-bit sequence is transmitted, it is always displayed on SEG1. Previous values are shifted to next display positions.

If 8-bit sequence is transmitted, it is shown on the right display (SEG1, SEG2), while previous value is shown on the left one.

If 16-bit sequence is transferred, it is shown on the display so that last bit (LSB) corresponds with least significant bit of SEG1.

If there are more than 16 bits transferred, the display will show last 16 bits received. Previous bits are ignored (lost).

6.2 3-wire mode, EN used as clock enable

If DIP switch EU=1 and EF=0, 3-wire mode with EN used as clock enable is selected.

This mode is especially suitable for such cases when CLK and DATA are connected to a bus shared with other devices. In desired moment the data is sent to bus while holding EN signal in active state so that INSIDER receives the data. After that INSIDER is disconnected by inverting the EN signal and the bus is available for other devices.

Clock is enabled according to EN polarity (EP DIP switch). If EP=0, the data is being received while EN=0. If EP=1 the data is being received while EN=1.

6.3 3-wire mode, EN is used as data strobe

If DIP switch EU=1 and EF=1, 3-wire mode with EN used as data strobe is selected. Data is continuously received by every period of CLK signal. The moment of data validity, when data is copied to display latch, is trigered by EN signal.

This mode is usefull especially when all INSIDER signals have to be shared with other application functions (e.g. CS - chip select).

The mode is also suitable for synchronous systems, where puls of a signal marks data validity. In this case CLK signal may be generated continuously, e.g. by a crystal oscilator.

The sense of EN signal depends on its polarity setting (switch EP). If EP=0 then EN=0 triggeres data transfer to latch while EN=1 causes last valid data to be kept. Similarily for EP=1.

7. CLK signal polarity settings

CP (Clock polarity) DIP switch determines the edge of CLK signal by whitch the data is transferred to shift register. In the moment of the transfer the data must

be stabble. It is recommended to change the data upon clock edge oposite to the one triggering the transfer.

If CP=0 the data is written to shift register upon falling edge of CLK signal. If CP=1 the data is written upon rising edge.

8. Status LED indicators

For better overview of the application and INSIDER state 4 status LEDs are provided.

PWR	green – power supply
DATA	red – indicates log.1 of DATA signal
CLK	red – indicates log.1 of CLK signal
EN	red – indicates log.1 of EN signal

9. Technical specification

inputs CMOS – 3 V, 5 V / TTL / LVT compatible			
inputs voltage log.1	Vih	2.2 V min.	max 5.5 V .
inputs voltage log.0	Vil	0 V min.	max 0.9 V .
frequency limit	fm		max 50 MHz .
input resistance	Rin	min. 1 MOhm	
input capacity	Cin		max 250 pF .
DC power supply of 9 V / 300 mA (adaptor is not part of the package) connection to application by cable with hooks			

10. Contact

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11. Functional schematics